AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph on page 1, lines 9-11, with the following amended paragraph:

This invention relates to a wiring structure of semiconductor device and particularly to a wiring structure suitable for VLSI and ULSI ~~USLI~~.

Please replace the paragraph on page 1, line 14, through page 2, line 1, with the following amended paragraph:

The speeding-up of silicon (Si) semiconductor is performed by reducing the device size to increase the integration density of transistors formed on the single-crystal Si substrate based on the ~~according to~~ Moore's Law. At present, the production of 0.13 μ m rule device has started. In 2005, it is planned to use ultra fine wiring with a width ~~thickness~~ of less than 0.10 μ m. A reduction in wiring width and wiring interval ~~due to the ultra fine process~~ causes an increase in electrical resistance of wiring and in inter-wiring capacity and, therefore, the wiring signal propagation speed decreases according as the ultra fine process makes progress. It is recognized especially after the 0.13 μ m rule that the problem of wiring delay adversely affects the operation speed of device. In the future development of Si semiconductor, the conversion of wiring material to new one is indispensable for increasing the wiring signal propagation speed since it is difficult to increase it by using the conventional ultra fine process.

Please replace the paragraph on page 2, lines 2-6, with the following amended paragraph:

The wiring delay can be reduced by using a wiring material with a resistivity lower than Al that is conventionally used as wiring material. In 1997, IBM Corp. ~~corp.~~,USA developed ~~proposed using~~ copper (Cu) wiring. The resistivity of bulk Cu is 1.7 $\mu\Omega \cdot$ cm while the resistivity of bulk Al is 2.7 $\mu\Omega \cdot$ cm.

Please replace the paragraph on page 6, lines 13-15, with the following amended paragraph:

FIG.2A is surface observation (SIM) images by focused ion beam (FIB) ~~FIB~~ showing the behavior of room temperature grain growth in a wiring structure of the invention;

Please replace the paragraph on page 7, lines 5-12, with the following amended paragraph:

A wiring structure in the preferred embodiment of the invention will be described below. The evaluation items are resistivity measurement by four-point probe, surface/cross section observation (SIM) images ~~(SIM image)~~ by focused ion beam (FIB), and crystal structure analysis by X-ray diffraction (XRD). Si substrate is used as the semiconductor, Si_3N_4 is formed on the Si substrate in order to observe the crystal grain of Cu film, and TiN is used as crystal grain promotion layer.

Please replace the paragraph on page 7, lines 13-29, with the following amended paragraph:

The Si substrate is cleaned ~~cleansed~~ by acetone and IPA, and then it is laid in a chamber of sputtering apparatus. Then, the chamber is highly vacuumed to 4 X 10^{-9} Torr, Ar of 8.5 CCM

and N_2 of 0.5 CCM are introduced therein, and Si_3N_4 of 60 nm thick is formed thereon using Si as target at a pressure of 5 X 10^{-3} Torr. Then, the chamber is highly vacuumed to 4 X 10^{-9} Torr, Ar of 8.5 CCM and N_2 of 0.5 CCM are introduced therein, and TiN, crystal promotion layer, of 0.1 μ m thick is formed thereon using Ti as target at a pressure of 5 X 10^{-3} Torr. Then, the chamber is highly vacuumed to 4 X 10^{-9} Torr, Ar of 10.0 CCM is introduced therein, and Cu, wiring layer, of 1.0 μ m thick is formed thereon using Cu as target at a pressure of 6 X 10^{-3} Torr. A comparative example without TiN layer is prepared. The property evaluation is conducted such that the behavior of grain growth at room temperature and after heat treatment of 2.5 hours at room at 350 °C in argon (Ar) atmosphere is evaluated with respect to the above evaluation items.

Please replace the paragraph on page 9, line 10, through page 10, line 4, with the following amended paragraph:

Although in the above embodiment of the invention the Si substrate is used as semiconductor, the same results are obtained in case of the Si substrate with SiO_2 formed thereon. It is obvious that the same effects will be obtained in case of having Si semiconductor layer (including impurity-doped layer and multiple layers) formed on the Si substrate and in case of further having SiO_2 film on that semiconductor layer. With regard to D (=average grain diameter of crystal grain)>10 x L (mean free path of electron), the average grain diameter of Cu may have no upper limit and it is desirable that the diameter becomes infinitely large to give a single crystal. Thereby, the scattering of electron due to crystal grain field can be reduced. It is desirable that the heat treatment is conducted in the range of 100 to 400 <u>°C, because,</u> ~~°C. Because,~~ in this range, the invention can have the significant effect. Although in the above

embodiment TiN, crystal grain promotion layer, of 0.1 μ m is formed, the crystal grain promotion layer does not have to be a uniform layer. Namely, even when it is 1 to 5 nm thick and grain-shaped or island-shaped without being combined, the crystal grain promotion function can be obtained. It is found that the same function or effect as TiN can be obtained in Ti, TiC, Ta, TaN and TaC. It is desirable that the dielectric film is of SiO_2 or organic material. The organic material may be formed porous.